a shallow region which extends to the surface of the substrate, the shallow region comprising:

a protective outer wall adjacent to the substrate;

an inner sealing wall located exclusively within the shallow region and adjacent to the protective outer wall: and

the shallow region having a shallow region cross-sectional area;

wherein the deep region cross-sectional area is greater than the shallow region cross-sectional area[, the deep region abutting only a single shallow region].

5. (Amended) A semiconductor isolation structure comprising:

a substrate, the substrate comprising a surface;

a first device and a second device formed within the substrate, each device in contact with the substrate;

an isolation region formed within the substrate between the first device and the second device, the isolation region comprising:

a deep region which extends into the substrate, the deep region comprising an oxide;

a shallow region which extends to the surface of the substrate, the shallow region comprising:

a protective outer wall adjacent to the substrate,

an inner sealing wall located exclusively within the shallow region and adjacent to the protective outer wall[; wherein the deep region abuts only a single shallow region].

A replacement copy of the claims is included following the Applicants' response.

EXAMINER'S REMARKS

Claims 1,2 and 4-6 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. patent No. 4,685,198 to Kawakita, et al (hereinafter Kawakita).